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| EXAMINER |
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| GOLDEN, JAMES R |

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Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No.<br>10/680,949 | Applicant(s)<br>HURLEY, WILLIAM M. | |
|---|---|---|---|
| | Examiner<br>James Golden | Art Unit<br>2187 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on 26 January 2006.
2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.
3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) 1-20 is/are pending in the application.
  4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5)☐ Claim(s) _____ is/are allowed.
6)☒ Claim(s) 1-20 is/are rejected.
7)☐ Claim(s) _____ is/are objected to.
8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.
10)☒ The drawing(s) filed on 08 October 2003 is/are: a)☒ accepted or b)☐ objected to by the Examiner.
  Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
  Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
  a)☐ All b)☐ Some * c)☐ None of:
    1.☐ Certified copies of the priority documents have been received.
    2.☐ Certified copies of the priority documents have been received in Application No. _____.
    3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
  * See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
  Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413)
  Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Response to Amendment*

This action is in response to the communication received January 26, 2006. Claims 1-20 are currently pending in the application.

### *Specification*

1. The corrections to the specification received on January 26, 2006 are accepted by the examiner, and the objections are withdrawn.

### *Claim Objections*

2. The corrections to claims 3 and 8 received on January 26, 2006 are accepted by the examiner, and the objections to claims 1-8 are withdrawn.

### *Claim Rejections - 35 USC § 102*

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. **Claims 1-2, 4-6, 9-10, 12-13 and 15-18** are rejected under 35 U.S.C. 102(b) as being anticipated by Joshi et al. (US 4,949,301).

5. **With respect to claim 1**, Joshi et al. disclose for use in a digital device (column 10, lines 1-7 discuss how data is composed of bits, which indicate it is a digital device), a first-in, first-out memory apparatus comprising:

- a memory operable to store a data packet (38 of Fig. 1; column 8, lines 41-51);
- circuitry operable to store the length of the data packet (128 and 134 of Fig. 6; column 2, lines 35-41; column 20, lines 18-22; column 26, lines 45-46) and the data packet (column 8, lines 41-44) in the memory; and
- circuitry operable to flush the length and the data packet from the memory when the data packet is invalid (column 27, line 61 -- column 28, line 20; although the flushing of the length of the data packet is not explicitly recited, the pointer for the next write is set to the address where packet reception started, and this will cause the length of the data and the data to be overwritten on the next write, which is "effectively flushing the data").

6. **With respect to claim 2**, Joshi et al. disclose the apparatus as set forth in claim 1 (see above paragraph 6) wherein:

- the length and data packet comprise a plurality of words (column 14, lines 55-57); and
- the circuitry for storing the length and data packet in the memory comprises a first pointer operable to identify a location in the memory (column 12, lines 62-64; column 23, line 67 -- column 24, line 10; the "WPR" pointer), wherein the first pointer is advanced for each word written to the memory (column 24, lines 10-14; column 25, lines 17-22).

7. **With respect to claim 4**, Joshi et al. disclose the apparatus as set forth in Claim 2 (see above paragraph 7), wherein the circuitry for flushing the length and data packet from the memory comprises an additional pointer operable to identify the first location in the memory where one of the words is stored, the location identified by the additional pointer being used as the first pointer when the data packet is flushed (column 23, lines 46-53; the "SWPR" pointer).

8. **With respect to claim 5**, Joshi et al. disclose the apparatus as set forth in claim 2 (see above paragraph 7), further comprising circuitry for retrieving the data packet from the memory (column 12, lines 60-62).

9. **With respect to claim 6**, Joshi et al. disclose the apparatus as set forth in claim 5 (see above paragraph 9), wherein the circuitry for retrieving the data packet comprises a second pointer operable to identify a location in the memory where a word is to be retrieved (column 12, lines 60-62; the "RPR" pointer).

10. **With respect to claim 9**, Joshi et al. disclose a digital device (column 10, lines 1-7 discuss how data is composed of bits, which indicate it is a digital device) comprising:

- at least one interface operable to receive and communicate data packets (22 of Fig. 1; column 7, lines 57-61); and
- a first-in, first-out memory comprising:
    - a memory operable to store a data packet (38 of Fig. 1; column 8, lines 41-51);

  - circuitry operable to store a length of the data packet (128 and 134 of Fig. 6; column 2, lines 35-41; column 20, lines 18-22; column 26, lines 45-46) and the data packet (column 8, lines 41-44) in the memory; and
  - circuitry operable to flush the length and the data packet from the memory when the data packet is invalid (column 27, line 61 -- column 28, line 20; although the flushing of the length of the data packet is not explicitly recited, the pointer for the next write is set to the address where packet reception started, and this will cause the length of the data and the data to be overwritten on the next write, which is "effectively flushing the data").

11. **With respect to claim 10**, Joshi et al. disclose the digital device as set forth in claim 9 (see above paragraph 11), wherein:

- the length and data packet comprise a plurality of words (column 14, lines 55-57); and
- the circuitry for storing the length and data packet in the memory comprises a first pointer operable to identify a location in the memory (column 12, lines 62-64; column 23, line 67 -- column 24, line 10; the "WPR" pointer), wherein the first pointer is advanced for each word written to the memory (column 24, lines 10-14; column 25, lines 17-22).

12. **With respect to claim 12**, Joshi et al. disclose the digital device as set forth in Claim 10 (see above paragraph 12), wherein the circuitry for flushing the length and data packet from the memory comprises an additional pointer operable to identify the first location in the memory where one of the words is stored, the location identified by

the additional pointer being used as the first pointer when the data packet is flushed (column 23, lines 49-53; the "SWPR" pointer).

13. **With respect to claim 13**, Joshi et al. disclose the digital device as set forth in claim 10 (see above paragraph 12), further comprising

- circuitry for retrieving the data packet from the memory (column 12, lines 60-62), the circuitry for retrieving the data packet comprising
- a second pointer operable to identify a location in the memory where a word is to be retrieved (column 12, lines 60-62; the "RPR" pointer).

14. **With respect to claim 15**, Joshi et al. disclose for use in a digital device (column 10, lines 1-7 discuss how data is composed of bits, which indicate it is a digital device), a method for storing data in a first-in, first-out memory, comprising:

- receiving a data packet (column 8, lines 41-44, lines 50-51);
- storing a length of the data packet (128 of Fig. 6; column 2, lines 35-41; column 20, lines 18-22; column 26, lines 45-46) and the data packet (column 8, lines 41-44) in the first-in, first-out memory (38 of Fig. 1; column 1, lines 50-52; column 8, lines 41-51); and
- flushing the length and the data packet from the memory when the data packet is invalid (column 27, line 61 -- column 28, line 20; although the flushing of the length of the data packet is not explicitly recited, the pointer for the next write is set to the address where packet reception started, and this will cause the length of the data and the data to be overwritten on the next write, which is "effectively flushing the data").

15. **With respect to claim 16**, Joshi et al. disclose the method as set forth in claim 15 (see above paragraph 15), wherein:

- the length and data packet comprise a plurality of words (column 14, lines 55-57); and
- the circuitry for storing the length and data packet in the memory comprises a first pointer operable to identify a location in the memory (column 12, lines 62-64; column 23, line 67 -- column 24, line 10; the "WPR" pointer), wherein the first pointer is advanced for each word written to the memory (column 24, lines 10-14; column 25, lines 17-22).

16. **With respect to claim 17**, Joshi et al. disclose the method as set forth in claim 16 (see above paragraph 16), wherein the circuitry for flushing the length and data packet from the memory comprises an additional pointer operable to identify the first location in the memory where one of the words is stored, the location identified by the additional pointer being used as the first pointer when the data packet is flushed (column 23, lines 46-53; the "SWPR" pointer).

17. **With respect to claim 18**, Joshi et al. disclose the method as set forth in claim 16 (see above paragraph 16), further comprising retrieving the data packet from the memory using a second pointer operable to identify a location in the memory where a word is to be retrieved (column 12, lines 60-62; the "RPR" pointer).

### *Claim Rejections - 35 USC § 103*

18. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

19. **Claims 3 and 11 are** rejected under 35 U.S.C. 103(a) as being unpatentable over Joshi et al. (US 4,949,301) as applied to claims 1-2, 4-6, 9-10, 12-13 and 15-18 above, and further in view of Epps et al. (US 6,778,546).

20. **With respect to claim 3**, Joshi et al. disclose the apparatus as set forth in claim 2 (see above paragraph 7).

Joshi et al. do not disclose expressly the limitation wherein the circuitry for storing the length and data packet further comprises:

- a length unit operable to provide the length of the data packet; and
- a multiplexer operable to selectively provide each of the length and the data packet to the memory.

However, Epps et al. disclose

- a length unit operable to provide the length of the data packet (column 1, lines 24-28); and
- a multiplexer operable to selectively provide each of the length and the data packet to the memory (470 of Figs. 4 and 11; column 6, lines 4-12 explains how data is separated into header and tail portions; column 7, lines 14-20 and column

15, lines 8-12 explain the function of the multiplexer; although it is not necessarily multiplexing between the packet length and packet data, the *n* bits of the header could be chosen so that this is the case).

Joshi et al. and Epps et al. are analogous art because they are from the same field of endeavor, namely packet forwarding and handling through a first-in, first-out memory.

At the time of invention, it would have been obvious to a person of ordinary skill in the art to combine the packet multiplexer of Epps et al. with the first-in first-out memory of Joshi et al. The motivation for doing so would have been "so that both the header and tail portions can be transmitted... over the same pins;" the multiplexer is further described as "a pin-saving mechanism" (column 7, lines 16-19).

Therefore, it would have been obvious to combine Epps et al. with Joshi et al. for the benefit of a first-in first-out memory with a multiplexer that transmits either the data packet length or the data packet to obtain the invention as specified in claim 3.

21. **With respect to claim 11**, Joshi et al. disclose the digital device as set forth in claim 10 (see above paragraph 12) wherein the circuitry for storing the length and data packet further comprises:

- a length unit operable to provide the length of the data packet (see above paragraph 6).

Joshi et al. do not disclose expressly the limitation wherein the circuitry for storing the length and data packet further comprises:

- a multiplexer operable to selectively provide each of the length and the data packet to the memory.

However, Epps et al. disclose

- a multiplexer operable to selectively provide each of the length and the data packet to the memory (470 of Figs. 4 and 11; column 6, lines 4-12 explains how data is separated into header and tail portions; column 7, lines 14-20 and column 15, lines 8-12 explain the function of the multiplexer; although it is not necessarily multiplexing between the packet length and packet data, the *n* bits of the header could be chosen so that this is the case).

Joshi et al. and Epps et al. are analogous art because they are from the same field of endeavor, namely packet forwarding and handling through a first-in, first-out memory.

At the time of invention, it would have been obvious to a person of ordinary skill in the art to combine the packet multiplexer of Epps et al. with the first-in first-out memory of Joshi et al. The motivation for doing so would have been "so that both the header and tail portions can be transmitted... over the same pins;" the multiplexer is further described as "a pin-saving mechanism" (column 7, lines 16-19).

Therefore, it would have been obvious to combine Epps et al. with Joshi et al. for the benefit of a first-in first-out memory with a multiplexer that transmits either the data packet length or the data packet to obtain the invention as specified in claim 3.

22. **Claims 7-8, 14 and 19-20 are** rejected under 35 U.S.C. 103(a) as being unpatentable over Joshi et al. (US 4,949,301) as applied to claims 1-2, 4-6, 9-10, 12-13 and 15-18 above, and further in view of Huang (US 5,311,475).

23. **With respect to claim 7**, Joshi et al. disclose the apparatus as set forth in claim 1 (see above paragraph 6).

Joshi et al. do not disclose expressly the limitations further comprising:

- a first counter operable to identify a number of data packets stored in the memory; and
- a second counter operable to identify a number of data packets retrieved from the memory.

However, Huang discloses the limitations further comprising:

- a first counter operable to identify a number of data packets stored in the memory (12 of Fig. 1a; column 1, lines 65-69; column 3, lines 55-59); and
- a second counter operable to identify a number of data packets retrieved from the memory (14 of Fig. 1a; column 1, lines 61-64; column 3, lines 55-59).

Joshi et al. and Huang are analogous art because they are from the same field of endeavor, namely first-in, first-out memories.

At the time of invention, it would have been obvious to a person of ordinary skill in the art to combine the write and read counters of Huang with the first-in, first-out memory of Joshi et al. The motivation for doing so would have been because the memory "includes a comparator for comparing the output of the two counters in order to determine whether the FIFO is empty or not" (column 1, lines 15-18); the comparator uses the counters to determine whether the FIFO is empty or not.

Therefore, it would have been obvious to combine Huang with Joshi et al. for the benefit of a first-in, first-out memory with write and read counters to obtain the invention as specified in claim 7.

24. **With respect to claim 8**, Joshi et al. disclose the apparatus as set forth in claim 7 wherein:

- the circuitry for storing the length and data packet in the memory comprises a first pointer (column 12, lines 62-64; column 23, line 67 -- column 24, line 10; the "WPR" pointer); and
- the apparatus further comprises:
  - circuitry for retrieving the data packet comprising a second pointer (column 12, lines 60-62; the "RPR" pointer);
  - a first comparator operable to compare outputs of the pointers and to generate a signal indicating that the memory is full when the outputs are equal (column 21, lines 31-41).

Joshi et al. do not disclose the limitation wherein

- a second comparator operable to compare outputs of the counters and to generate a signal indicating the memory is empty when the outputs are equal.

However, Huang discloses

- a second comparator operable to compare outputs of the counters and to generate a signal indicating the memory is empty when the outputs are equal (16 of Fig. 1a; column 5, lines 16-26).

Joshi et al. and Huang are analogous art because they are from the same field of endeavor, namely first-in, first-out memories.

At the time of invention, it would have been obvious to a person of ordinary skill in the art to combine the comparator of Huang with the write and read counters of Huang and the first-in, first-out memory of Joshi et al. The motivation for doing so would have been because the memory "also includes a comparator for comparing the output of the two counters in order to determine whether the FIFO is empty or not" (column 1, lines 15-18).

Therefore, it would have been obvious to combine Huang with Joshi et al. for the benefit of a first-in, first-out memory with a comparator attached to the write and read counters to obtain the invention as specified in claim 7.

25. **With respect to claim 14**, Joshi et al. disclose the digital device as set forth in Claim 9 (see above paragraph 11), wherein:

- the circuitry for storing the length and data packet in the memory comprises a first pointer (column 12, lines 62-64; column 23, line 67 -- column 24, line 10; the "WPR" pointer); and
- the digital device further comprises:
  - circuitry for retrieving the data packet comprising a second pointer (column 12, lines 60-62; the "RPR" pointer);

  - a first comparator operable to compare outputs of the pointers and to generate a signal indicating that the memory is full when the outputs are equal (column 21, lines 31-41).

Joshi et al. do not disclose the limitation wherein the digital device further comprises

- a first counter operable to identify a number of data packets stored in the memory;
- a second counter operable to identify a number of data packets retrieved from the memory; and
- a second comparator operable to compare counters and to generate a signal indicating the memory is empty when the outputs are equal.

However, Huang discloses

- a first counter operable to identify a number of data packets stored in the memory (12 of Fig. 1a; column 1, lines 65-69; column 3, lines 55-59) ; and
- a second counter operable to identify a number of data packets retrieved from the memory (14 of Fig. 1a; column 1, lines 61-64; column 3, lines 55-59).

Joshi et al. and Huang are analogous art because they are from the same field of endeavor, namely first-in, first-out memories.

At the time of invention, it would have been obvious to a person of ordinary skill in the art to combine the write and read counters of Huang with the first-in, first-out memory of Joshi et al. The motivation for doing so would have been because the memory "also includes a comparator for comparing the output of the two counters in order to determine whether the FIFO is empty or not" (column 1, lines 15-18) the comparator uses the counters to determine whether the FIFO is empty or not.

Huang also discloses

- a second comparator operable to compare outputs of the counters and to generate a signal indicating the memory is empty when the outputs are equal (16 of Fig. 1a; column 5, lines 16-26).

At the time of invention, it would have been obvious to a person of ordinary skill in the art to combine the comparator of Huang with the write and read counters of Huang and the first-in, first-out memory of Joshi et al. The motivation for doing so would have been because the memory "also includes a comparator for comparing the output of the two counters in order to determine whether the FIFO is empty or not" (column 1, lines 15-18).

Therefore, it would have been obvious to combine Huang with Joshi et al. for the benefit of a first-in, first-out memory with write and read counters and an attached comparator to obtain the invention as specified in claim 14

26. **With respect to claim 19**, Joshi et al. disclose the method as set forth in claim 15 (see above paragraph 15).

Joshi et al. do not disclose expressly the limitations further comprising:

- incrementing a first counter for each data packet stored in the memory; and
- incrementing a second counter for each data packet retrieved from the memory.

However, Huang discloses the limitations further comprising:

- incrementing a first counter for each data packet stored in the memory (12 of Fig. 1a; column 3, lines 55-59); and
- incrementing a second counter for each data packet retrieved from the memory (14 of Fig. 1a; column 1, lines 64-65; column 3, lines 55-59).

Joshi et al. and Huang are analogous art because they are from the same field of endeavor, namely first-in, first-out memories.

At the time of invention, it would have been obvious to a person of ordinary skill in the art to combine the write and read counters of Huang with the first-in, first-out memory of Joshi et al. The motivation for doing so would have been because the memory "also includes a comparator for comparing the output of the two counters in order to determine whether the FIFO is empty or not" (column 1, lines 15-18); the comparator uses the counters to determine whether the FIFO is empty or not.

Therefore, it would have been obvious to combine Huang with Joshi et al. for the benefit of a first-in, first-out memory with write and read counters to obtain the invention as specified in claim 7.

27. **With respect to claim 20**, Joshi et al. disclose the method as set forth in claim 19 (see above paragraph 27), wherein:

- storing the length and data packet in the memory comprises using a first pointer (column 12, lines 62-64; column 23, line 67 -- column 24, line 10; the "WPR" pointer); and
- further comprising:

- retrieving the data packet from the memory using a second pointer (column 12, lines 60-62; the "RPR" pointer);
- comparing outputs of the pointers and generating a signal indicating that the memory is full when the outputs are equal (column 21, lines 31-41).

Joshi et al do not disclose expressly the limitation further comprising:

- comparing outputs of the counters and generating a signal indicating the memory is empty when the outputs are equal.

However, Huang discloses

- a second comparator operable to compare outputs of the counters and to generate a signal indicating the memory is empty when the outputs are equal (16 of Fig. 1a; column 5, lines 16-26).

Joshi et al. and Huang are analogous art because they are from the same field of endeavor, namely first-in, first-out memories.

At the time of invention, it would have been obvious to a person of ordinary skill in the art to combine the comparator of Huang with the write and read counters of Huang and the first-in, first-out memory of Joshi et al. The motivation for doing so would have been because the memory "also includes a comparator for comparing the output of the two counters in order to determine whether the FIFO is empty or not" (column 1, lines 15-18).

Therefore, it would have been obvious to combine Huang with Joshi et al. for the benefit of a first-in, first-out memory with a comparator attached to the write and read counters to obtain the invention as specified in claim 20.

### *Response to Arguments*

28. **With respect to applicant's argument regarding the rejections of claims 1, 9 and 15** (pages 11-12 of applicant's remarks), Joshi et al. teaches that the data packet is effectively flushed when the status bit is zero (column 28, lines 16-20, as noted in the First Action dated 10/26/2005). The applicant argues "Since the status and length of the packet have not been recorded at the time the packet is flushed, it is clear that the length is not flushed with the packet" (page 12, lines 4-6). However, the data packet is not overwritten when it is "effectively flushed"; it is marked invalid by the status bit that reads zero. Therefore, the byte that holds status and length information does not have to be overwritten in order to be considered effectively flushed also. When the packet has a status bit that reads zero, the data packet is effectively flushed, and the packet (and in addition the status and length byte) will be overwritten on the next write (the data packet is written into memory locations 2-100 in steps 1-4 of Fig. 8, as in column 25, line 13 -- column 26, line 44, especially column 26, lines 30-44; the status and length byte is written into memory location 1, as in column 26, lines 61-66; the write pointer is moved to overwrite the packet and status and length byte, column 28, lines 2-3). This rejection stands as issued.

29. **With respect to applicant's argument regarding the rejections of claims 3 and 11** (page 12 of applicant's remarks), these rejections stand as issued; see above paragraph 28 for a detailed explanation.

## *Conclusion*

30. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

31. Any inquiry concerning this communication or earlier communications from the examiner should be directed to James R. Golden whose telephone number is 571-272-5628. The examiner can normally be reached on Monday-Friday, 8:30 AM - 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on 571-272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

James R. Golden
Patent Examiner
Art Unit 2187

April 3, 2006

Brian R. Peugh
Primary Examiner
AU 2187
4/10/06